LISTING OF CLAIMS:

1. (Previously presented) A semiconductor device having a thin film resistance element located above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects to the surface of the semiconductor substrate is set to be within a range that is greater than 0° and less than or equal to 10°.

2. (Original) The semiconductor device according to claim 1, wherein the interlayer insulating film comprises an inorganic spin-on-glass film formed so as to cover the overall area below the area where the thin film resistance element is formed.

3. (Original) The semiconductor device according to claim 1, wherein the interlayer insulating film comprises an inorganic spin-on-glass film, and wherein an upper surface of the interlayer insulating film has a higher area adjacent to an area where the thin film resistance element is formed than in the area where the thin film resistance element is not formed.

4. (Original) The semiconductor device according to claim 1, wherein the thin film resistance element is formed on an area where the wire is formed, and a wire interval is set to 1.7μm or more.

5. (Original) The semiconductor device according to claim 1, wherein the thin film resistance element is formed above the area where the wire is formed, and the thin film resistance element and the wire are disposed in parallel to each other so that projections thereof are overlapped with each other.

6. (Previously presented) A semiconductor device having a thin film resistance element located above an interlayer insulating film above an area where at least one of an element and a wire is formed, wherein the interlayer insulting film comprises an inorganic spin-on-glass film formed so as to cover the overall area below an area where the thin film resistance element is formed.

7. (Withdrawn) A method of manufacturing the semiconductor device of claim 6, the method comprising:

rotationally coating an inorganic spin-on-glass film to form the inorganic spin-on-glass film as the interlayer insulating film above the area while flattening the upper surface of the inorganic spin-on-glass film; and

forming any one of the thin film resistance element and an insulating film constituting the interlayer insulating film on the inorganic spin-on-glass film flattened by the rotational coating.

8. (Withdrawn) A method of manufacturing a semiconductor device having a thin film resistance element through an interlayer insulating film above an area where at least one of an element and a wire is formed, the method comprising:

rotationally coating an inorganic spin-on-glass film to form the inorganic spin-on-glass film as the interlayer insulating film above the area while flattening the upper surface of the inorganic spin-on-glass film; and

forming any one of the thin film resistance element and an insulating film constituting the interlayer insulating film on the inorganic spin-on-glass film flattened by the rotational coating.

9. (Previously presented) A semiconductor device having a thin film resistance element disposed above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects to the surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°, wherein the interlayer insulating film comprises an inorganic spin-on-glass film formed so as to cover the overall area below the area where the thin film resistance element is formed, wherein the thin film resistance element is formed on an area where the wire is formed, and a wire interval is set to 1.7μm or more.

10. (Previously presented) The semiconductor device according to claim 9, wherein the thin film resistance element is formed to have a width in a range between 1 and 10μm, and a thickness in a range between 10 and 50nm.

11. (Previously presented) The semiconductor device according to claim 3, wherein the thin film resistance element is formed to have a width in a range between 1 and 10μm, and a thickness in a range between 10 and 50nm.

12. (Previously presented) A semiconductor device having a thin film resistance element disposed above an interlayer insulating film above an area where a plurality of wires is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects to the surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°, wherein the interlayer insulating film comprises an inorganic spin-on-glass film, wherein a wire interval is set to 1.7μm or more.

13. (New) The semiconductor device according to claim 1, wherein the thin film resistance element further comprises paired thin film resistance elements.

14. (New) The semiconductor device according to claim 1, further comprising a plurality of the thin film resistance element, wherein the area where at least one of the element and the wire is formed below each of the plurality of thin film resistance elements is identical.

15. (New) The semiconductor device according to claim 1, wherein the thin film resistance element further comprises paired thin film resistance elements, wherein the area where

at least one of the element and the wire is formed below each of the paired thin film resistance elements is identical.